WHAT IS CLAIMED IS:

1. An AGC circuit, comprising:

a variable gain amplifier circuit having a gain controlled by a gain control signal,

a rectification circuit that rectifies an output signal of said variable gain amplifier circuit,

a first voltage comparator that compares a rectified signal rectified by said rectification circuit with an arbitrarily preset voltage,

a first up/down counter that switches between the up-count operation and the down-count operation in accordance with the level of the output voltage of said first voltage comparator, and

a first D/A conversion circuit that outputs a voltage corresponding to the count value of said first up/down counter,

wherein it is adapted so that a gain control signal corresponding to the voltage output from said first D/A conversion circuit is supplied to said variable gain amplifier circuit.

2. The AGC circuit according to claim 1, wherein a first up-count operation clock and a first down-count operation clock are input separately into said first up/down counter.

3. The AGC circuit according to claim 1, wherein a first register is provided between said first voltage comparator and said first up/down counter, the output voltage of said first

voltage comparator is stored in said first register at a cycle of a first reference clock, the up-count operation and the down-count operation of said first up/down counter is switched in accordance with the level of the voltage stored in said first register, thereby it is adapted so that any changes of the output voltage of said first voltage comparator within a period shorter than the cycle of said first reference clock is not transmitted to said first up/down counter.

4. The AGC circuit according to claim 1, wherein a first count operation control circuit is provided between said first voltage comparator and said first up/down counter, the output voltage of said first voltage comparator is transmitted to said first up/down counter or the transmission thereof is shut down in accordance with the count value of said first up/down counter by said first count operation control circuit, and thereby the count value of said first up/down counter is restricted within a range from a predetermined first upper limit value to a predetermined first lower limit value.

5. The AGC circuit according to claim 3, wherein a first count operation control circuit is provided between said first register and said first up/down counter, the output voltage of said first register is transmitted to said first up/down counter or the transmission thereof is shut down in accordance with the count value of said first up/down counter by said first count operation control circuit, and thereby the count value of said

first up/down counter is restricted within a range from a predetermined first upper limit value to a predetermined first lower limit value.

6. The AGC circuit according to claim 1, wherein said first up/down counter has a function to execute the up-count operation or to stop the execution thereof in accordance with the count value, and to execute the down-count operation or to stop the execution thereof in accordance with the count value, thereby the count value is restricted within a range from a predetermined first upper limit value and a predetermined first lower limit value.

7. An AGC circuit, comprising:

a variable gain amplifier circuit having a gain controlled by a gain control signal,

a rectification circuit that rectifies an output signal of said variable gain amplifier circuit,

a first voltage comparator that compares a rectified signal rectified by said rectification circuit with an arbitrarily preset voltage,

a first up/down counter that switches between the up-count operation and the down-count operation in accordance with the level of the output voltage of said first voltage comparator,

a first D/A conversion circuit that outputs a voltage corresponding to the count value of said first up/down counter,

a second up/down counter,

a second D/A conversion circuit that outputs a voltage corresponding to the count value of said second up/down counter,

a second voltage comparator that compares the output voltage of said first D/A conversion circuit with the output voltage of said second D/A conversion circuit, and

a changeover circuit that outputs the higher output voltage of the output voltage of said first D/A conversion circuit and the output voltage of said second D/A conversion circuit based on the level of the output voltage of said second voltage comparator,

wherein it is adapted so as to switch between the up-count operation and the down-count operation of the second up/down counter according to the level of the output voltage of said second voltage comparator, thereby a gain control signal corresponding to the voltage output from said changeover circuit is supplied to said variable gain amplifier circuit.

8. The AGC circuit according to claim 7, wherein a first up-count operation clock and a first down-count operation clock are input separately into said first up/down counter, and a second up-count operation clock and a second down-count operation clock are input separately into said second up/down counter.

9. The AGC circuit according to claim 7, wherein a first register is provided between said first voltage comparator and

said first up/down counter, the output voltage of said first voltage comparator is stored in said first register at a cycle of a first reference clock, the up-count operation and the down-count operation of said first up/down counter is switched in accordance with the level of the voltage stored in said first register, and it is adapted so that any changes of the output voltage of said first voltage comparator within a period shorter than the cycle of said first reference clock is not transmitted to said first up/down counter.

10. The AGC circuit according to claim 9, wherein a second register is provided between said second voltage comparator and said second up/down counter and said changeover circuit, the output voltage of said second voltage comparator is stored in said second register at a cycle of a second reference clock, the up-count operation and the down-count operation of said second up/down counter is switched in accordance with the level of the voltage stored in said second register, and it is adapted so that any changes of the output voltage of said second voltage comparator within a period shorter than the cycle of said second reference clock is not transmitted to said second up/down counter.

11. The AGC circuit according to claim 7, wherein a first count operation control circuit is provided between said first voltage comparator and said first up/down counter, the output voltage of said first voltage comparator is transmitted to said

first up/down counter or the transmission thereof is shut down in accordance with the count value of said first up/down counter by said first count operation control circuit, and thereby the count value of said first up/down counter is restricted within a range from a predetermined first upper limit value to a predetermined first lower limit value, and

a second count operation control circuit is provided between said second voltage comparator and said second up/down counter, the output voltage of said second voltage comparator is transmitted to said second up/down counter or the transmission thereof is shut down in accordance with the count value of said second up/down counter by said second count operation control circuit, and thereby the count value of said second up/down counter is restricted within a range from a predetermined second upper limit value to a predetermined second lower limit value.

12. The AGC circuit according to claim 10, wherein a first count operation control circuit is provided between said first register and said first up/down counter, the output voltage of said first register is transmitted to said first up/down counter or the transmission thereof is shut down in accordance with the count value of said first up/down counter by said first count operation control circuit, and thereby the count value of said first up/down counter is restricted within a range from a predetermined first upper limit value to a predetermined first

lower limit value, and

a second count operation control circuit is provided between said second register and said second up/down counter, the output voltage of said second register is transmitted to said second up/down counter or the transmission thereof is shut down in accordance with the count value of said second up/down counter by said second count operation control circuit, and thereby the count value of said second up/down counter is restricted within a range from a predetermined second upper limit value to a predetermined second lower limit value.

13. The AGC circuit according to claim 7, wherein said first up/down counter has a function to execute the up-count operation or to stop the execution thereof in accordance with the count value, and to execute the down-count operation or to stop the execution thereof in accordance with the count value, thereby to restrict the count value within a range from a predetermined first upper limit value and a predetermined first lower limit value, and

said second up/down counter has a function to execute the up-count operation or to stop the execution thereof in accordance with the count value, and to execute the down-count operation or to stop the execution thereof in accordance with the count value, thereby to restrict the count value within a range from a predetermined second upper limit value and a predet rmined second lower limit value.